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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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SALIWANCHIK LLOYD & SALIWANCHIK
A PROFESSIONAL ASSOCIATION
PO BOX 142950
GAINESVILLE, FL 32614-2950

EXAMINER	
JEFFERSON, QUOVAUNDA	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 09/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/747,601	KEUM, DONG YEAL	
	Examiner	Art Unit	
	Quovaunda Jefferson	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 2* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 2* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huang-Lu et al, US Patent Application Publication 2001/0044191 in view of Hong et al, US Patent 5,614,746.

Regarding claim 1, Huang-Lu teaches a method for fabricating a transistor comprising of forming a gate electrode **302** on a semiconductor substrate **300**, forming a first preliminary source/drain region and a pocket junction region **312** through a first ion implantation process **310** using the gate electrode as a mask, the pocket junction region being formed under the first preliminary source/drain region, forming a nitride layer **302** with on the first oxide layer **304**, forming a second oxide layer (layer that forms **314**) over the nitride layer, forming spacers **314** on sidewalls of the gate electrode, forming a second preliminary source/drain region through a second ion implantation **316** process using the spacers as a mask (Figure 3D), and diffusing

substantially all of the implanted ions in a horizontal direction of the substrate by performing a thermal treatment process for the resulting substrate [0010].

Huang-Lu fails to teach forming a first oxide layer on the substrate including the gate electrode and removing the nitride layer and the first oxide layer on the surface of the substrate.

Hong teaches forming a first oxide layer on the substrate including the gate electrode (Hong teaches an oxide-nitride-oxide spacer, which is constructed by forming a first oxide layer, a nitride layer over the first oxide and a second oxide layer over the nitride layer to form a ONO layer **38**, columns 5 and 6) and removing the nitride layer and the first oxide layer on the surface of the substrate (Figure 3E-The ONO layer is etched off the substrate to form the spacers) as a method for forming ONO spacers, which protect the gate electrode.

It would be obvious to one skilled in the art to combine the teachings of Hong with that of Huang-Lu because Hong provides a method for forming ONO spacers, which protect the gate electrode.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huang-Lu and Hong as applied to claim 1 above, and further in view of Xiang et al, US Patent 6,555,439.

Regarding claim 2, Huang-Lu and Hong fail to teach performing a thermal treatment process prior to the removal of the nitride layer and the first oxide layer.

Xiang teaches comprising performing a thermal treatment process prior to the removal of the nitride layer and the first oxide layer (column 5, lines 31-36) because annealing is conducted to activate source/drain extensions and to recrystallize extensions.

It would have been obvious to one skilled in the art to combine the teachings of Xiang with that of Huang-Lu and Hong because annealing is conducted to activate source/drain extensions and to recrystallize extensions.

Response to Arguments

Applicant's arguments filed June 22, 2006 have been fully considered but they are not persuasive. Applicant argues that Hong fails to teach "forming a first oxide layer on the substrate, including a gate electrode, forming spacers on the sidewalls of the gate electrode, and then removing the nitride layer and the first oxide layer on the surface of the substrate" as stated in claim 1.

In regards to the argument that Hong fails to teach "forming a first oxide layer on the substrate, including a gate electrode", Applicant states that "the ONO spacers of Hong are formed on a gate oxide layer".

In response to the argument that Hong shows the formation of the ONO spacer on the gate oxide layer and not the substrate, the Examiner would like to point out that the both the gate oxide layer **22** and the spacer layer **38** of Hong are on the substrate **20**, as shown in Figures 3D and 3E. While the spacer layer **38** and the substrate **20** are not in direct contact with one another, Hong does disclose that ONO layer **38** is indeed on the substrate **20**. Therefore, Hong does teach this limitation as set forth by Applicant's claim 1.

In regards to the argument that Hong fails to teach "forming spacers on the sidewalls of the gate electrode, and then removing the nitride layer and the first oxide layer on the surface of the substrate", Applicant states that the first oxide layer and the nitride layer are removed in a single etching step during forming the spacers on the sidewalls of the gate electrode. Applicant further contends that Hong teaches "deposition of a first oxide layer, a nitride layer, and a second oxide layer on a thin oxide layer, then performing an anistropic etch of the entire ONO to form an ONO spacer".

In response to the argument, Examiner would like to point out that there were no limitations set forth in the claim that the first oxide and first nitride layers are each

removed in separate steps nor that **only** the first oxide layer and first nitride layer was removed from the surface of the substrate. Indeed, as pointed out by Applicant and Hong, Figure 3E, Hong teaches removal of the gate oxide layer, first oxide layer, first nitride layer, **and** second oxide layer on the surface of the semiconductor substrate. Therefore, Hong also teaches this limitation as set forth by Applicant's claim 1.

Applicant argues that the cited references combined fail the claim invention. In particular, since Hong "fails to teach or suggest forming spacers on the sidewall of the gate electrode separate from removing the nitride layer and the first oxide layer on the surface of the substrate such that forming a second preliminary source/drain region through a second ion implantation process using the spacers as a mask can occur without removing the nitride layer and the first oxide layer on the surface and the first oxide layer on the surface of the substrate".

In response to this argument, Examiner is confused as to what is being argued in this point. Examiner thinks that Applicant meant to say that the second ion implantation process can't occur without removing the layers on the surface of the substrate. Regardless, as stated before, Hong teaches that teaches removal of the gate oxide layer, first oxide layer, first nitride layer, **and** second oxide layer on the surface of the semiconductor substrate in figure 3E. Also, Huang-Lu teaches a second ion implantation process, using spacer **214** as a mask, but keeps the nitride layer **208** on

the substrate. Therefore, Hong also teaches this limitation as set forth by Applicant's claim 1.

Regarding claim 2, Applicant argues that Xiang fails to teach "forming a first oxide layer on the substrate, including a gate electrode, forming spacers on the sidewalls of the gate electrode, and then removing the nitride layer and the first oxide layer on the surface of the substrate". In response to this argument, Examiner points out that these limitations are taught by Hong, as discussed previously.

Therefore, the rejections of claims 1 and 2 as unpatentable over Huang-Lu et al in view of Hong et al and Xiang et al is deemed proper.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quovaunda Jefferson whose telephone number is 571-272-5051. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

QVJ

MICHELLE ESTRADA
PRIMARY EXAMINER